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Code No. : 15454 H

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E. : Honours) V-Semester Main Examinations, Jan./Feb.-2024

FPGA Based System Design

Time: 3 hours

Max. Marks: 60

Note: Answer all questions from Part-A and any FIVE from Part-B

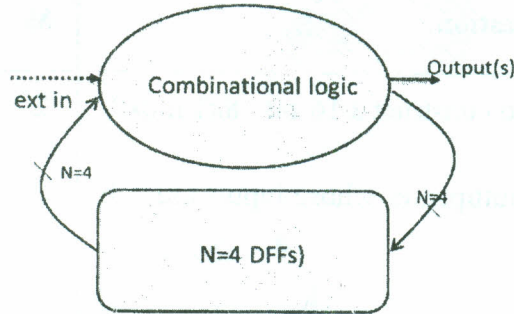
Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO	PSO
1.	How many 1-bit 2x1 muxes are required to construct a 16-bit 8x1 mux?	2	1	1	1	1
2.	Write a logical expression for a 4-input multiplexer whose inputs are a, b, c, d and select lines are s1 and s0.	2	2	1	1	1
3.	All bits of an 8-bit number $a_7a_6a_5a_4a_3a_2a_1a_0$ are fed to a logic circuit which has an output, plnd . When the 8-bit input is the same as seen in forward and reverse direction, plnd becomes 1. Write the logical expression for plnd .	2	2	1	2	1
4.	Write a simple, but complete Verilog module which causes the output y to become 1, only when all the bits of an 8-bit input a are at logic-1. In all other cases, y is 0.	2	1	1	1	1
5.	A sequential circuit has M states. (i) How many flipflops are required in the design if one-hot encoding is used? (ii) How many flipflops are required if binary encoding is used?	2	2	2	2	1
6.	What is the extra logic circuitry in an asynchronous FIFO which is not required in synchronous FIFO?	2	1	2	1	1
7.	In the context of IC packages, expand the following acronyms: PGA, BGA, FBGA, QFP.	2	1	4	1	1
8.	What are the main programmable resources in an FPGA?	2	1	4	1	1
9.	What are the main types of FPGA, based on programming type?	2	1	5	1	1
10.	In the implementation of a logic design on the FPGA (using Vivado), in which step will we get an error if the constraints file is not included?	2	1	5	1	1

Contd... 2

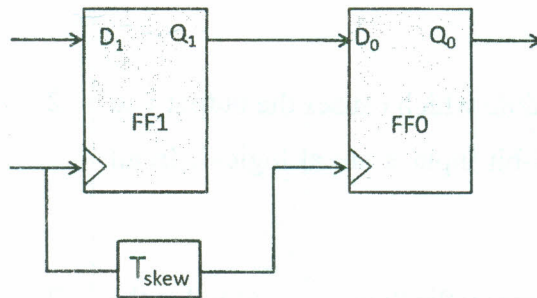
Part-B (5 × 8 = 40 Marks)

11. a) In a certain finite state machine, whose structure is shown in the following figure, 4 flip flops are used. The combinational circuit part of the state machine has a worst-case delay of 2.25ns, while **each** D flipflop has a setup time of 0.63ns, a hold time of 0.25ns, and a clock to Q delay of 0.8ns. Clock jitter is 20ps. What is the highest frequency at which the circuit can run correctly? Give your answer in Megahertz, rounded off to the nearest integer.



4 2 1 3 1

- b) Each D-flipflop in the following circuit has a setup time of 0.6ns, clock-to-Q delay of 0.9ns and a hold time of 0.2ns. What kind of timing violation can possibly occur in the circuit below, and when will such a timing violation occur?



4 2 1 2 1

12. a) Define a Verilog module for a FULL ADDER (FA) at the dataflow level (using operators &, |, ^). Using only FA modules, write a Verilog module named *rca_4* for a 4-bit ripple carry adder which adds TWO 4-bit numbers, *a*[3:0] and *b*[3:0].

3 3 2 2 1

- b) (i) Write a complete Verilog module named *decade_counter* that is used as a frequency divider. The *synchronous* counter counts from 0 to 9 in steps of 1, and then repeats the sequence. Use *clk* as the input clock and *rst* as the reset. Use active-low asynchronous reset. The signal *clkout* is the output clock.

5 3 2 3 1

13. a) Why is one-hot encoding of states used in FSMs despite needing more flip flops than those needed in binary encoding of states?

2 2 3 1 1

- b) Write a complete Verilog module (Test bench is NOT needed) for a MEALY style FSM that detects a 5-bit sequence 10110. Overlapping sequences must be detected. You **MUST** use **two** always blocks in the Verilog code – one for the next-state logic and one for the sequential elements. The output signal *detect* must go high whenever the above sequence is observed. *clk* is the clock and *rst* is the asynchronous, active low reset signal. Use binary encoding for the states.

6 3 2 1 1

14. a)	What are the main functions of an I/O pad in an FPGA?	3	1	4	2	1
b)	Implement the function $F = \sum (1,4,7,8,10,15,18,21,25,28,31)$ using a 5-variable LUT, constructed from 4-variable LUTs.	5	3	4	3	1
15. a)	(i) What is the main programmable logic element at the heart of a CLB? (ii) How many logical functions can be implemented from 4 variables?	4	2	5	1	1
b)	Draw a flow diagram showing the different steps in the generation of a bit file when using the Vivado software. Explain briefly each step.	4	2	5	2	1
16. a)	An 8-to-3 priority encoder has data inputs in <u>decreasing</u> order of priority as follows: D7, D6, D5, D4, D3, D2, D1, D0. It has a single bit output V which is 1 if any one or more bits are asserted. Write the <u>simplified</u> logic equations for the priority outputs P2, P1, P0 and for the output V.	4	3	1	3	1
b)	Assuming that FULL ADDER / HALF ADDER blocks are available to you, draw a diagram to show how you will add 8 one-bit numbers a, b, c, d, e, f, g, h. Show the connections clearly.	4	3	2	2	1
17.	Answer any <i>two</i> of the following:					
a)	Describe in a few lines, how the fifo_full signal is generated in an asynchronous FIFO.	4	2	3	1	1
b)	The EDA tool vendor Synopsys supplies to the VLSI world, the ASIC synthesis tool called DC (Design Compiler). (i) Why does Synopsys not provide an FPGA synthesis tool, like Vivado? (ii) What information is present in the 'constraints' file used in the implementation of your logic design on an FPGA?	4	2	4	1	1
c)	An FPGA board from Xilinx has an onboard 100MHz clock and 4 seven-segment LED displays. You are required to design a 2-digit BCD counter that displays the seconds on 2 LED displays. This BCD counter requires a 1-Hz clock which is derived from 100MHz. Starting from 100MHz clock, how many flipflops (minimum) are needed for the counter and frequency divider?	4	4	5	3	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%
